REMARKS

Claims 1, 2, 4-15 and 17-23 are all the claims pending in the application. Claims 1, 7, and 15 are the independent claims. Applicants offer the following remarks for the examiner's consideration.

35 U.S.C. §102(b) Rejections

Claims 1, 2, 4-15 and 17-23 are rejected under 35 U.S.C. §102(b), as being anticipated by U.S. Patent No. 5,420,992 to Killian *et al.*

Killian *et al.* does not anticipate each feature of independent claims 1, 7, and 15. For example, the independent claims each recite an "address format control signal" to indicate zero-extension or sign-extension of an address reference.

An embodiment of the presently disclosed invention enables operation using both signed and unsigned virtual address spaces. *See, e.g.,* page 2, line 25 to page 3, line 2. This is accomplished through the address format control flag 114, which indicates the type of virtual address space utilized. If the address space control flag 112 indicates a confined-address space, then the address format control flag 114 is checked to see whether the virtual address space is signed or unsigned. If the address space is unsigned, zero-extension is used, while if the address space is signed, sign extension is used.

In comparison, Killian only discloses a signed *address* space. While Killian does disclose selecting between sign extension and zero extension depending upon which particular instruction is loaded (*see* col. 10, lines 1-4, *discussing* prior art; col. 13, lines 10-18, *discussing* Table 3A), no such selection is made for *addresses*. Whether to sign extend or zero extend a particular instruction is determined by a look-up table (col. 12, line 66 to col. 13, line 4), whereas the address space in Killian is sign extended or zero extended without consideration of the virtual memory format employed. *See, e.g.,* Killian col. 3, line 64 to col. 4, line 7 ("In m-bit user mode, it is necessary to sign-extend the address when two's complement overflow occurs. A straightforward approach for the m-bit mode is to provide sign-extension hardware in the virtual address path to guarantee a sign-extended output in the event of m-bit two's complement

overflow. However, where timing constraints militate against such sign-extension, it suffices to force the (N-m) most significant bits to zero. Accordingly, in one embodiment, zeroing circuitry is provided in the path to the address translation unit.").

In view of the above, applicants respectfully submit that Killian *et al.* does not anticipate at least the address format aspect of the invention recited in the independent claims, as the virtual address space in Killian *et al.* is all signed. In Killian *et al.*, whether to choose zero-extension or sign extension for the address space is a question depending upon timing constraints considered when designing the address translation unit, not on the format of a particular address. Accordingly, the address format control signal having a first setting to indicate zero-extension and a second setting to indicate sign-extension is not anticipated. Reconsideration and withdrawal of the § 102(b) rejection are requested.

Additionally, dependent claim 11 recites generation of an address fault flag based at least in part on a comparison of the generated address reference (of the second bit size; *see* claim 7) and the extended, truncated, generated address reference (also of the second bit size; *see* claim 7). This feature is not disclosed in Killian *et al.* Killian *et al.* discloses a check of twos-complement overflow, as alluded to by the examiner in paragraph 14 of the Office Action. However, this check is performed before the address is sign-extended, as the results are used to decide whether address sign-extension will even be performed. *See, e.g.*, Killian *et al.* col. 3, lines 64-66. No comparison is made between the N-bit address before sign extension and after truncation/sign extension. Similar features are recited in claims 4 and 22. Reconsideration is requested.

Conclusion

In view of the above remarks, reconsideration and allowance of all claims are requested.

Applicants authorize the Commissioner to charge any fees determined to be due under 37 C.F.R. § 1.16 or § 1.17 or credit any overpayment to Deposit Account No. 11-0600.

The Examiner is invited to contact the undersigned at (202) 220-4209 to discuss any matter concerning this application.

Respectfully submitted,

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Dated: October 4, 2004

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